August 2000 FAIRCHILD SEMICONDUCTOR IM FDR8321L P-Channel MOSFET With Gate Driver For Load Switch Application **General Description** Features • $V_{\text{DROP}} = 0.2V @ V_{\text{IN}} = 5V$, $I_{\text{L}} = 2.9A$. $R_{\text{DS(ON)}} = 0.070 \ \Omega$ This device is designed for configuration as a load switch and is particularly suited for Power $V_{\text{DROP}} = 0.2V @ V_{\text{IN}} = 2.5V, I_{\text{L}} = 2A. R_{\text{DS(ON)}} = 0.105 \ \Omega.$ Management in portable battery powered electronic V_{ON/OFF} Zener protection for ESD ruggedness (>6KV Human equipment. Designed to operate from 2.5V to 8V input Body Model). and supply up to 2.9A. The device features a small N-Channel MOSFET (Q1) together with a large P-Channel power MOSFET (Q2) in a single SuperSOT[™]-8 package. • High density cell design for extremely low on-resistance. SuperSOT[™]-8 SOT-23 SOIC-16 SuperSOT[™]-6 SO-8 SOT-223 EQUIVALENT CIRCUIT .c₁.c₀ 5 4 VIN,R1,Ci -Vout, C1, Co 6 3 R1,R2,C1 VDROP ... о и т 7 2 C1,Co R2 R₂ 8 1 VON/OFF ON/OFF O-SuperSOT[™]-8 See Application Circuit Absolute Maximum Ratings T₄ = 25°C unless otherwise noted Symbol Parameter FDR8321L Units V_{IN} Input Voltage Range 2.5 - 8 V On/Off Voltage Range 1.5 - 8 V_{ON/OFF} V Load Current @ V_{DROP}= 0.2V - Continuous \mathbf{I}_{L} 2.9 А (Note 1) 10 - Pulsed P_{D} Maximum Power Dissipation 0.8 W (Note 2) $\mathsf{T}_{\mathsf{J}},\mathsf{T}_{\mathsf{STG}}$ Operating and Storage Temperature Range -55 to 150 ℃ THERMAL CHARACTERISTICS $\mathsf{R}_{\theta JA}$ Thermal Resistance, Junction-to-Ambient °C/W 156 (Note 2) 40 °C/W Thermal Resistance, Junction-to-Case $R_{\theta JC}$ (Note 2)

| Electrical Characteristics (T _A = 25°C unless otherwise noted) | | | | | | | | |
|---|--|--|-----|-------|-------|-------|--|--|
| Symbol | Parameter | Conditions | Min | Тур | Max | Units | | |
| OFF CHA | RACTERISTICS | | • | | | | | |
| I _{FL} | Forward Leakage Current | $V_{IN} = 5 \text{ V}, V_{ONOFF} = 0 \text{ V}$ | | | 1 | μA | | |
| ON CHAR | ACTERISTICS (Note 3) | | | | | | | |
| VDROP | Conduction Voltage Drop | $V_{IN} = 5 \text{ V}, V_{ONOFF} = 3.3 \text{ V}, I_{L} = 2.9 \text{ A}$ | | 0.185 | 0.2 | V | | |
| | | $V_{IN} = 2.5 \text{ V}, V_{ONOFF} = 3.3 \text{ V}, I_{L} = 2 \text{ A}$ | | 0.18 | 0.2 | | | |
| R _{DS(ON)} | Q ₂ - Static Drain-Source On-Resistance | $V_{GS} = -5 \text{ V}, \ I_{D} = -2.9 \text{ A}$ | | 0.06 | 0.07 | Ω | | |
| | | $V_{GS} = -2.5 \text{ V}, I_{D} = -2 \text{ A}$ | | 0.09 | 0.105 | | | |
| I _L | Load Current | $V_{DROP} = 0.2 \text{ V}, V_{IN} = 5 \text{ V}, V_{ON/OFF} = 3.3 \text{ V}$ | 2.9 | | | Α | | |
| | | $V_{\text{DROP}} = 0.2 \text{ V}, V_{\text{IN}} = 2.5 \text{ V}, V_{\text{ONOFF}} = 3.3 \text{ V}$ | 2 | | | | | |

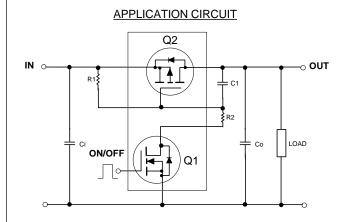
Notes:

1. V_{IN} =5V, $V_{ON/OFF}$ =8V, V_{DROP} =0.2V, T_A =25°C

R_{b,k} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{b,k} is guaranteed by design while R_{b,k} is determined by the user's board design. R_{b,k} typical =156°C/W when mounted on a minimum 0.0025 in² pad on FR-4.

3. Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2.0%

FDR8321L Load Switch Application

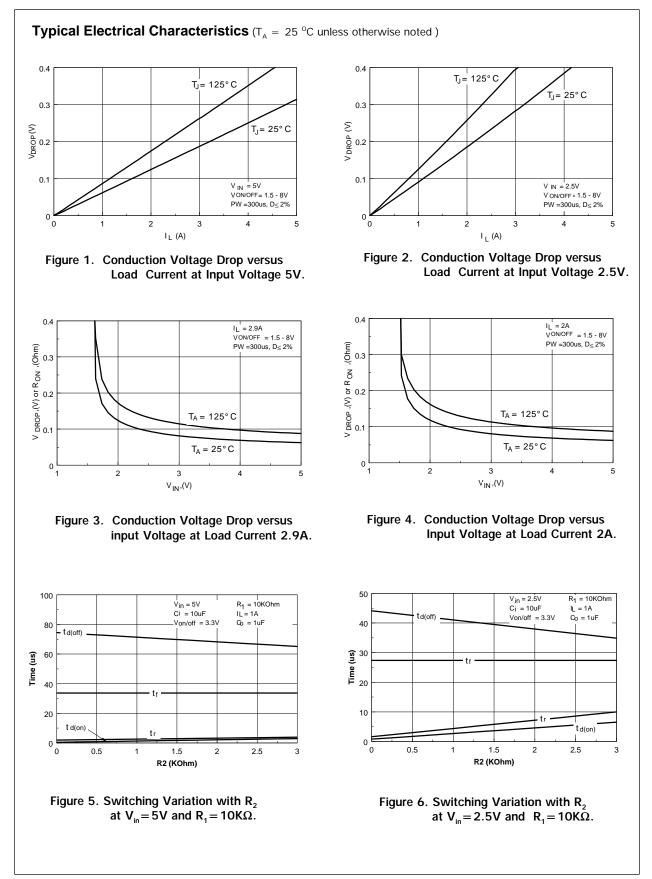


External Component Recommendation

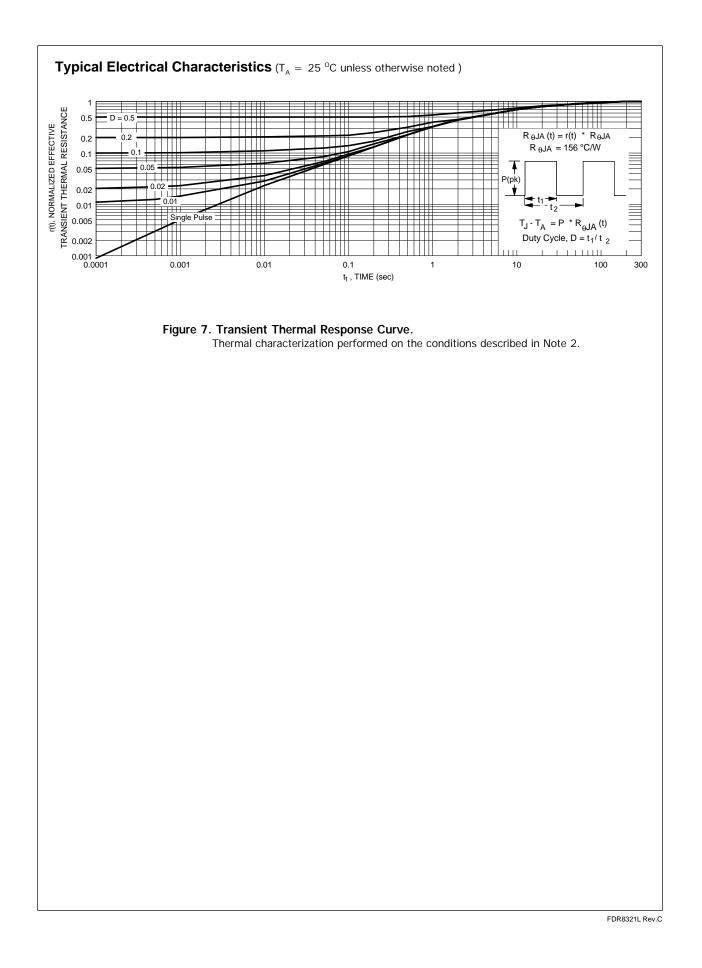
First select R2, 100 - $1k\Omega$, for Slew Rate control.

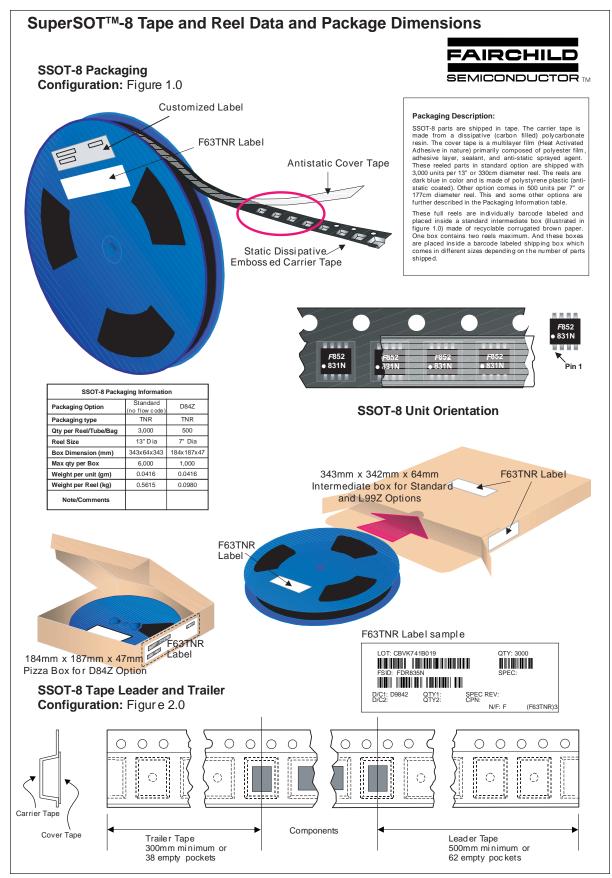
 $C1 \le 1000 pF$ can be added in addition to R2 for further In-rush current control.

Then select R1 such that R1/R2 ratio maintains between 10 - 100. R1 is required to turn Q2 off. For SPICE simulation, users can download a "FDR8321L.MOD" Spice model from Fairchild Web Site at www.fairchildsemi.com

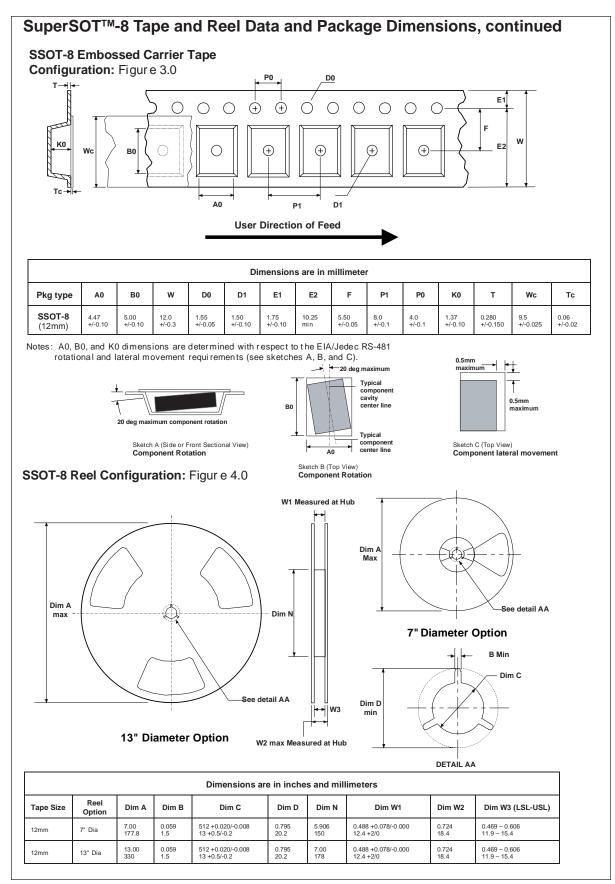


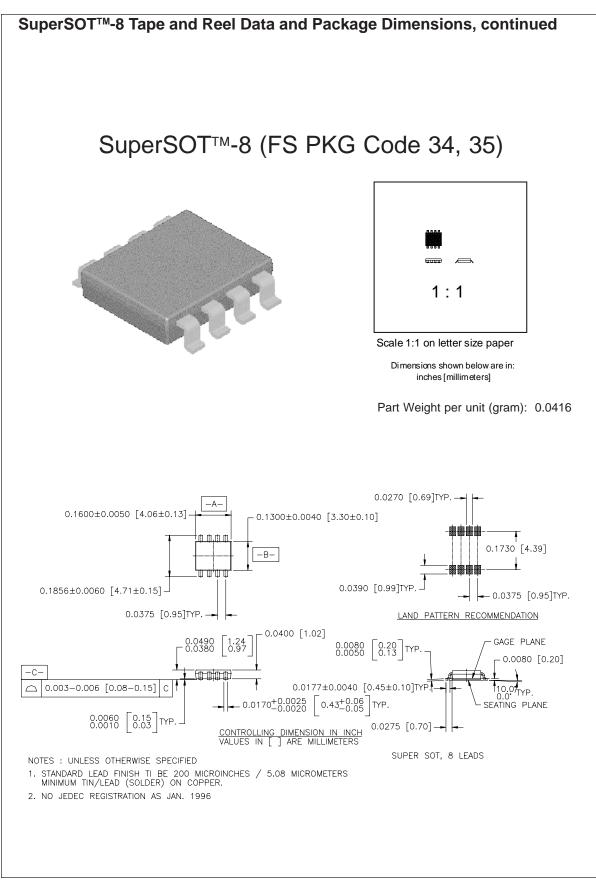
FDR8321L Rev.C





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